CLAIMS

What is claimed is:

1. An electronic processing boot up system comprising:

a bus for communicating information;

a processor coupled to said bus, said processor for processing said information; and

a read only memory (ROM) emulation system coupled to said bus, said read only memory (ROM) emulation system for making boot up information available to said processor.

2. An electronic processing system of Claim 1 wherein said read only memory (ROM) emulation system comprises:

a NAND flash memory for storing said boot up information; and

a controller component for generating commands for retrieving boot up information from said NAND flash and forwarding said boot up information to said processor.

3. An electronic processing system of Claim 1 wherein said controller component includes a field programmable gate array.

4. An electronic processing system of Claim 1 further comprising a state machine for holding off said processor while assembling an instruction stream on the fly for retrieving said boot up information from said NAND flash memory and sending said boot up information to said processor.

5. An electronic processing system of Claim 4 wherein commands generated by said state machine are compatible with a NAND flash memory protocol for retrieving information.

6. An electronic processing system of Claim 1 wherein said read only memory (ROM) emulation system permits reprogramming and recovery after a system crash.

7. An electronic processing system of Claim 1 further comprising a joint task action group (JTAG) port for directly controlling electrical signals in said electronic processing boot up system to effect programming of said NAND flash memory with system software.

8. An electronic processing boot up method comprising:

initiating an initial memory fetch;

performing a read only memory (ROM) emulation process; and

passing control to an operating system.

9. An electronic processing boot up method of Claim 8 wherein said read only memory (ROM) emulation process comprises:

receiving a fetch request for information from a processor;

translating said fetch request into memory compatible commands for retrieving said information;

holding off said processor while said information is retrieved; and

forwarding said information in a format compatible with a reply to said memory fetch.

10. An electronic processing boot up method of Claim 8 wherein said holding off said processor includes implementation of a ready handshake protocol.

11. An electronic processing boot up method of Claim 8 wherein said ready handshake protocol includes:

de-assert a ready signal in response to said fetch request; and

asserting a ready signal when said information is in a format compatible with a reply to said memory fetch.

12. An electronic processing boot up method of Claim 8 wherein said memory compatible commands are compatible with a NAND flash memory.

13. An electronic processing boot up method of Claim 8 wherein a ready handshake protocol is initialized.

14. An electronic processing boot up method of Claim 8 wherein said translating includes translating a read only memory (ROM) memory access fetch request into NAND flash compatible commands.

15. An electronic processing boot up method of Claim 8 further comprising turning on random access memory (RAM) and copying information from a NAND flash memory to said random access memory (RAM), wherein said information includes bootstrap information.

16. An electronic processing boot up method of Claim 15 wherein balance of bootstrap information is retrieved from random access memory (RAM).

17. An electronic processing boot up method of Claim 15 bad pages of a NAND flash memory are marked and skipped when copying information from said NAND flash.

18. A read only memory emulation system comprising:

a non-volatile memory for storing boot up instructions; and

an controller component for interfacing between said non-volatile memory and a processor.

19. A read only memory emulation system of Claim 18 wherein said non-volatile memory is a NAND flash memory.

20. A read only memory emulation system of Claim 18 wherein said controller component converts fetch cycle operations of said processor into said non-volatile memory access operations.

21. A read only memory emulation system of Claim 18 further comprising a volatile memory for receiving boot up instructions from said non-volatile memory and completing a bootstrap sequence.

22. A read only memory emulation system of Claim 18 further comprising a volatile memory for receiving boot up instructions from said non-volatile memory and completing a bootstrap sequence.

23. A read only memory emulation system of Claim 18 wherein said controller component includes a field programmable gate array component.